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EXAMINER	
SONG, JASMINE	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,109	ERLANDSON ET AL.	
	Examiner	Art Unit	
	Jasmine Song	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 07/16/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This office action is in response to amendment filed on 07/16/2004. Claims 1-38 are pending in the application. All rejections and objections not explicitly repeated below are withdrawn.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 38 is rejected under 35 U.S.C. 102(e) as being anticipated by Fukuyama et al., U.S 2002/0110037 A1.

Regarding claim 38, Fukuyama teaches that a memory, comprising:

an address bus (Fig.7, the address bus 11) operable to receive an external address (address signals shown in Fig.7, such as the burst-starting address 000000000/01/000000, col.7, section 0105) during a data-transfer cycle (data access within SDRAM);

an address counter (Fig.7, address counter 42) operable to generate an internal address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000) during the data-transfer cycle (col.7 to col.8, section 0105 to section 0108);

an address decoder (Fig.7, address decoder 21) coupled to the address counter;

a comparator (Fig.7, burst column address comparator 45) coupled to the address bus and to the address counter and operable to compare the external address (col.6, section 0091) to the internal address (it is taught as the first counting up from an initial seventeen-bit count value of 000000000/01/000000, col.8, 0107); and

a control circuit (Fig.7, active/precharge command generator 44) coupled to the comparator (burst column address comparator 45) and operable to enable a data transfer (active/precharge command generator 44 enable and disable the issuance of read and write command to access SDRAM as shown in Fig.7, col.6 to col.7, section 0091-0092) based on the relationship between the external address and the internal address (Fig.7, col.6 to col.7, section 0091 to 0092).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 1-17 and 20-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuyama et al., U.S 2002/0110037 A1, in view of Biggs., U.S. Patent 6,128,716.

Regarding claim 1, Fukuyama teaches that a memory, comprising:

an address bus (Fig.7, the address bus 11) operable to receive an external address (address signals shown in Fig.7, such as the burst-starting address 000000000/01/000000, col.7, section 0105) during a data-transfer cycle (data access within SDRAM);

an address counter (Fig.7, address counter 42) operable to generate an internal address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000) during the data-transfer cycle (col.7 to col.8, section 0105 to section 0108);

an address decoder (Fig.7, address decoder 21) coupled to the address counter;

a comparator (Fig.7, burst column address comparator 45) coupled to the address bus and operable to compare the external address (col.6, section 0091) to a value (a value is taught as the page-stop value, as well as the ending or final column address in the specification from page 6 to page 10); and

a control circuit (Fig.7, active/precharge command generator 44) coupled to the comparator (burst column address comparator 45) and operable to enable and disable a data transfer (active/precharge command generator 44 enable and disable the issuance of read and write command to access SDRAM as shown in Fig., col.6 to col.7, section 0091-0092) based on the relationship between the external address and the value(Fig.7, col.6, section 0091).

Fukuyama does not teach terminating a data-transfer cycle based on the relationship between the external address and the value.

However, Biggs teaches terminating a data-transfer cycle (it is taught as terminating the page mode access by deactivating both RAS and CAS) based on the relationship between the external address and the value (it is taught as R2 is not equal to R3, col.4, lines 66 to col.5, lines 5).

As taught by Biggs, terminating a data-transfer cycle based on the relationship between the external address and the value has the advantages of allowing the precharge to start early and avoids the precharge penalty of the full page mode (col.2, lines 18-19 and col.4, lines 10-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Biggs in the system of Fukuyama and terminating a data-transfer cycle based on the relationship between the external address and the value for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated

one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 2, Fukuyama teaches that the address bus (Fig.7, the address bus 11) is operable to receive an external column address (burst-starting row/bank/column address 000000000/01/0000000); and the address counter (Fig.7, address counter 42) is operable to generate an internal column address (col.8, lines 0116 such as 000000000/01/000001).

Regarding claim 3, Fukuyama teaches that the address bus is operable to receive an initial external address (burst-starting row/bank/column address 000000000/01/0000000) and a subsequent external address (col.8, lines 0116); and

the address counter is operable to store the initial external address (col.7, section 0105, last two lines) and to generate the internal address by varying the stored initial external address (col.8, lines 0107).

Regarding claim 4, Fukuyama teaches that the address bus is operable to receive an initial external address (burst-starting row/bank/column address 000000000/01/0000000) and a subsequent external address (col.8, lines 0116); and the address counter is operable to store the initial external address(col.7, section 0105, last two lines), to generate an initial internal address equal to the stored initial external address (it is taught as the first counting up from an initial seventeen-bit count value of

000000000/01/000000, col.8, 0107), and to generate a subsequent internal address by varying the stored initial external address (col.8, lines 0107).

Regarding claim 5, Fukuyama teaches that the address bus is operable to receive an initial external address and a subsequent external address; and

the address counter is operable to store the initial external address, to generate an initial internal address equal to the stored initial external address (it is taught as the first counting up from an initial seventeen-bit count value of 000000000/01/000000, col.8, 0107), and to generate a subsequent internal address equal to the subsequent external address by varying the stored initial external address (col.8, lines 0107).

Regarding claims 6 and 8, Fukuyama teaches that further comprising:

a data buffer (it is taught as one of rows within the same bank in the SDRAM);

wherein the comparator (Fig.7, comparator 45) is coupled to the address counter (address counter 42) and is operable to compare (col.6, section 0091) the external address (the burst-starting address) to the internal address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000); and

wherein the control circuit (Fig.7, active/precharge command generator 44) is coupled to the data buffer and the address counter (Fig.7) and is operable to enable the data buffer and the counter if the external address equals the internal address and to

disable the data buffer if the external address does not equal the internal address (col.3, section 0050 to col.4, section 0053).

Regarding claims 7 and 9, Fukuyama teaches that further comprising:

a data buffer (it is taught as one of rows within the same bank in the SDRAM);

a storage circuit (read/write command generator 43, col.8, section 0108, last three lines) operable to store a predetermined address (it is taught as the last row/bank/column address);

wherein the comparator is coupled to the storage circuit and is operable to compare the external address (the burst-starting row/bank/column address) to the predetermined address; and

wherein the control circuit is coupled to the data buffer and the address counter and is operable to enable the data buffer and the counter (it is taught as the burst busy signal 51 to the high level to indicate that a burst operation has begun; col.8, section 0109) if the external address does not equal the predetermined address and to disable the counter if the external address equals the predetermined address (col.8, section 0109).

Regarding claim 10, Fukuyama teaches that the data-transfer cycle comprises a read cycle (col.8, section 0114).

Regarding claim 11, Fukuyama teaches that a memory, comprising:

a data buffer operable to receive and hold data during a data transfer cycle (it is taught as one of rows within the same bank in the SDRAM);

an address counter (Fig.7, address counter 42) operable to generate an internal address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000) during the data-transfer cycle (col.7 to col.8, section 0105 to section 0108);

a programmable storage circuit (read/write command generator 43, col.8, section 0108, last three lines) operable to store a value (it is taught as the last row/bank/column address) during the data transfer cycle; and

a control circuit coupled to the storage circuit and the data buffer and operable to disable the data transfer cycle in response to the value (col.8, section 0109).

Fukuyama does not teach terminating the data-transfer cycle in response to the value.

However, Biggs teaches terminating the data-transfer cycle (it is taught as terminating the page mode access by deactivating both RAS and CAS) in response to the value (it is taught as R3, col.4, lines 66 to col.5, lines 5).

As taught by Biggs, terminating the data-transfer cycle in response to the value has the advantages of allowing the precharge to start early and avoids the precharge penalty of the full page mode (col.2, lines 18-19 and col.4, lines 10-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Biggs in the system of Fukuyama and terminating a data-transfer cycle in response to the value for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 12, Fukuyama teaches that the control circuit is operable to disable the address counter (col.8, lines 0109, last two lines) in response to the value.

Regarding claim 13, Fukuyama teaches that wherein the control circuit is operable to disable the data buffer in response to the value (burst operation has ended; col.8, lines 0109, last two lines).

Regarding claim 14, Fukuyama teaches that the programmable storage circuit (read/write command generator 43, col.8, section 0108, last three lines) comprises a programmable counter operable to generate a count by incrementing or decrementing the stored value during the data-transfer cycle (col.8, section 0108, last four lines); and

wherein the control circuit is operable to terminate the data transfer when the count equals a predetermined value (col.8, section 0109, last three lines).

Regarding claim 15, Fukuyama teaches that further comprising:

wherein the programmable storage circuit (read/write command generator 43, col.8, section 0108, last three lines) is operable to store an address value (it is taught as the last row/bank/column address);

a comparator (Fig.7, burst column address comparator 45) coupled to the address counter, the storage circuit, and the control circuit and operable to compare the internal address (the address generated by the address counter based on the burst-starting address 000000000/01/000000) to the address value; and wherein the control circuit is operable to terminate the data transfer when the internal address has a predetermined relationship to the address value (col.8, section 0109).

Regarding claim 16, Fukuyama teaches that the address counter is operable to generate an internal column address (col.8, lines 0116 such as 000000000/01/000001).

Regarding claim 17, Fukuyama teaches that wherein the address counter is operable to store an initial internal address (col.7, section 0105, last two lines) and to generate a subsequent internal address by incrementing or decrementing the stored initial internal address (col.8, lines 0107).

Regarding claim 20, Fukuyama teaches that an electronic system, comprising:

a data input device (Fig.1);

a data output device (Fig.1); and

a computer circuit (the microprocessor) coupled to the data input and output devices and including a processor and a memory circuit coupled to the processor (Fig.1, col.2, section 0028), the memory circuit including,

an address counter (Fig.7, address counter 42) operable to generate an internal address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000) during a data transfer cycle between the processor and the memory (col.7 to col.8, section 0105 to section 0108);

a storage circuit (read/write command generator 43, col.8, section 0108, last three lines) operable to receive and store a value (it is taught as the last row/bank/column address) from the processor before or during the data transfer cycle; and a control circuit coupled to the storage circuit and operable to disable the data transfer cycle in response to the stored value (col.8, section 0109).

Fukuyama does not teach terminating the data-transfer cycle in response to the stored value.

However, Biggs teaches terminating the data-transfer cycle (it is taught as terminating the page mode access by deactivating both RAS and CAS) in response to the stored value (it is taught as R3, col.4, lines 66 to col.5, lines 5).

As taught by Biggs, terminating the data-transfer cycle in response to the stored value has the advantages of allowing the precharge to start early and avoids the precharge penalty of the full page mode (col.2, lines 18-19 and col.4, lines 10-12). It would have been obvious to one having ordinary skill in the art at the time the invention

was made to utilize the teachings of Biggs in the system of Fukuyama and terminating a data-transfer cycle in response to the stored value for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 21, Fukuyama teaches that the storage circuit (read/write command generator 43, col.8, section 0108, last three lines) comprises a programmable counter operable to generate a count by incrementing or decrementing the stored value during the data transfer cycle (col.8, section 0108, last four lines); and

wherein the control circuit is operable to terminate the data transfer when the count equals a predetermined value (col.8, section 0109, last three lines).

Regarding claim 22, Fukuyama teaches that the value stored in the storage circuit comprises an address value (it is taught as the last row/bank/column address);

the memory further includes a comparator (Fig.7, burst column address comparator 45) coupled to the address counter, the storage circuit, and the control circuit and operable to compare the internal address (the address generated by the address counter based on the burst-starting address 000000000/01/000000) to the address value; and wherein the control circuit is operable to terminate the data transfer

cycle when the internal address has a predetermined relationship to the address value (col.8, section 0109).

Regarding claim 23, Fukuyama teaches that a method, comprising:

receiving a first address (address signals shown in Fig.7, such as the burst-starting address 000000000/01/000000, col.7, section 0105);

generating a second address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000);

comparing (Fig.7, burst column address comparator 45) the first address(col.6, section 0091) to the second address (a value is taught as the page-stop value, as well as the ending or final column address in the specification from page 6 to page 10); and

Fukuyama does not teach terminating a cycle during which data is being transferred to or from a storage location residing at the second address if the first address does not have a predetermined relationship to the second address.

However, Biggs teaches terminating a cycle during which data is being transferred to or from a storage location residing at the second address (it is taught as terminating the page mode access by deactivating both RAS and CAS) if the first address does not have a predetermined relationship to the second address (it is taught as R2 is not equal to R3, col.4, lines 66 to col.5, lines 5).

As taught by Biggs, terminating a cycle during which data is being transferred to or from a storage location residing at the second address if the first address does not have a predetermined relationship to the second address has the advantages of

allowing the precharge to start early and avoids the precharge penalty of the full page mode (col.2, lines 18-19 and col.4, lines 10-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Biggs in the system of Fukuyama and terminating a cycle during which data is being transferred to or from a storage location residing at the second address if the first address does not have a predetermined relationship to the second address for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 25, Fukuyama teaches that receiving a first address comprises receiving with a memory circuit a first address that is generated outside of the memory circuit (it is taught as external address received by the bus 11); and generating a second address comprises generating a second address inside of the memory circuit (it is taught as internal address generated by address counter).

Regarding claims 24 and 26, Biggs teaches that terminating the cycle comprises terminating the cycle if the first address does not equal the second address; and enabling the cycle if the first address equals the second address (col.4, lines 60 to col.5, lines 5).

Regarding claim 27, Fukuyama teaches that a method, comprising:

generating a first address (address signals shown in Fig.7, such as the burst-starting address 000000000/01/000000, col.7, section 0105);

comparing (Fig.7, burst column address comparator 45) the first address (col.6, section 0091) to a predetermined value address (a value is taught as the page-stop value, as well as the ending or final column address in the specification from page 6 to page 10); Fukuyama does not teach terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value.

However, Biggs teaches terminating a cycle during which data is being transferred to or from a storage location residing at the first address (it is taught as terminating the page mode access by deactivating both RAS and CAS) if the first address has a predetermined relationship to the predetermined value (it is taught as R3, col.4, lines 66 to col.5, lines 5).

As taught by Biggs, terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value has the advantages of allowing the precharge to start early and avoids the precharge penalty of the full page mode (col.2, lines 18-19 and col.4, lines 10-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Biggs in the system of Fukuyama and terminating a cycle during which data is being

transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 28, Fukuyama teaches that further comprising enabling the cycle if the first address does not have the predetermined relationship to the predetermined value (col.8, section 0091).

Regarding claim 29, Fukuyama teaches that wherein generating a first address comprises generating the first address inside of a memory circuit (it is taught as internal address generated by address counter).

Regarding claim 30, Fukuyama teaches that wherein generating a first address comprises generating the first address outside of a memory circuit (it is taught as external address received by the bus 11).

Regarding claim 31, Fukuyama teaches further comprising disabling the cycle comprises disabling the cycle if the first address equals the predetermined value; and

enabling the cycle if the first address does not equal the predetermined value (col.8, section 0109).

Regarding claim 32, Fukuyama teaches that further comprising

wherein generating a first address comprises generating the first address inside of a memory circuit (it is taught as internal address generated by address counter); and

receiving with the memory circuit a second address from outside of the memory circuit (it is taught as external address received by the bus 11).

Regarding claim 33, Fukuyama teaches that further comprising loading the predetermined value into a memory that includes the storage location (read/write command generator 43, col.8, section 0108, last three lines).

Regarding claim 34, Fukuyama teaches that a method, comprising:

loading a memory (SDRAM) with a count value from an external source(col.8, section 0107 such as 000000000/01/000000);

generating a first address inside of the memory, the first address being distinct from the count value (it is taught as internal address generated by address counter, col.7, section 0092, lines 6-9);

incrementing or decrementing the count value (col.8, section 0107 to 0108);

comparing (Fig.7, burst column address comparator 45) the count value (col.6, section 0091) to a predetermined value (a value is taught as the page-stop value, as well as the ending or final column address in the specification from page 6 to page 10, such as final column address 111111 as taught as in col.6, section 0091); and

Fukuyama does not teach terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value.

However, Biggs teaches terminating a cycle during which data is being transferred to or from a storage location residing at the first address (it is taught as terminating the page mode access by deactivating both RAS and CAS) if the first address has a predetermined relationship to the predetermined value (it is taught as R3, col.4, lines 66 to col.5, lines 5).

As taught by Biggs, terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value has the advantages of allowing the precharge to start early and avoids the precharge penalty of the full page mode (col.2, lines 18-19 and col.4, lines 10-12). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Biggs in the system of Fukuyama and terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the first address has a predetermined relationship to the predetermined value for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 35, Fukuyama teaches that further comprising disabling the transferring of data to or from the storage location if the first address does not have the predetermined relationship to the predetermined value(col.8, section 0109).

Regarding claim 36, Fukuyama teaches that wherein transferring data comprises:

terminating the cycle comprises terminating the cycle if the count value equals the predetermined value (col.8, section 0109); and

enabling the cycle if the count value does not equal the predetermined value (col.8, section 0109).

Regarding claim 37, Fukuyama teaches that further comprising receiving with the memory a second address from outside of the memory while generating the first address (it is taught as external address received by the bus 11).

7. Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuyama et al., U.S 2002/0110037 A1, in view of Kim., U.S. Patent 6484231 B1.

Regarding claims 18 and 19, Fukuyama teaches that an electronic system, comprising:

a data input device (Fig.1);

a data output device (Fig.1); and

a computer circuit (the microprocessor) coupled to the data input and output devices and including a processor and a memory circuit coupled to the processor (Fig.1, col.2, section 0028), the memory circuit including,

an address bus (Fig.7, the address bus 11) operable to receive an external address (address signals shown in Fig.7, such as the burst-starting address 000000000/01/000000, col.7, section 0105) during a data-transfer cycle (data access within SDRAM);

an address counter (Fig.7, address counter 42) operable to generate an internal address (the address 000000001/01/000000 generated by the address counter based on the burst-starting address 000000000/01/000000) during the data-transfer cycle (col.7 to col.8, section 0105 to section 0108);

an address decoder (Fig.7, address decoder 21) coupled to the address counter;

a comparator (Fig.7, burst column address comparator 45) coupled to the address bus and operable to compare the external address (col.6, section 0091) to a value (a value is taught as the page-stop value, as well as the ending or final column address in the specification from page 6 to page 10); and

a control circuit (Fig.7, active/precharge command generator 44) coupled to the comparator (burst column address comparator 45) and operable to enable a data

transfer (active/precharge command generator 44 enable to access SDRAM as shown in Fig.7) based on the relationship between the external address and the value(Fig.7, col.6, section 0091).

Fukuyama does not disclose a multiplexer, specifically disclose that a multiplexer coupled to the address bus, the address counter, and the address decoder and operable to couple either the external address or the internal address to the address decoder during the data transfer.

However, Kim disclose a multiplexer (Fig.4, multiplexer 100), and the multiplexer coupled to the address bus (address signals go to address register 1), the address counter (counter 40), and the address decoder (decoder 50) and operable to couple either the external address (address before address register 1) or the internal address (address after decoder) to the address decoder during the data transfer (Fig.4).

As taught by Kim, the use of the multiplexer coupled to the address bus, the address counter, and the address decoder and operable to couple either the external address or the internal address to the address decoder during the data transfer has the advantages of receiving a plurality of selected cell data from the output circuit in accordance with the coding signal from the counter and outputs the plurality of selected cell data, therefore, the operation speed of the memory chip is increased (col.3, lines 44-45 and col.4, lines 35-39). It would have been obvious to one having ordinary skill in the art at the time the invention was made to utilize the teachings of Kim in the system of Fukuyama and have the multiplexer coupled to the address bus, the address counter, and the address decoder and operable to couple either the external address or the

internal address to the address decoder during the data transfer for the advantages stated above.

Accordingly, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Response to applicant's Arguments

8. Applicant's arguments with respect to claims 1-17 and 20-37 have been considered but are moot in view of the new ground(s) of rejection.

9. Applicant's arguments filed 07/16/2004 regarding to claim 18-19 have been fully considered but they are not persuasive.

10. In response to applicant's argument that Kim discloses a multiplexer 100, this multiplexer does not couple any address to the address decoder 50, however, it is noticed that this limitation is taught in Fig. 4, an address decoder 50 receives an external address signal ADD from the address register 1 and a burst mode signal BMS from the control unit 3 for generating an internal address signal (col.5, lines 66 to col.6, lines 2), the generated internal address coupled to the multiplexer as shown in Fig.4, the applicant does not claim directly coupled to address bus, therefore, broadly written claims are disclosed by the reference cited.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

13. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Mano Padmanabhan
10/18/04

Jasmine Song
Patent Examiner
October 18, 2004

Mano Padmanabhan
Supervisory Patent Examiner
Technology Center 2100

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER